REMARKS

The rejections presented in the Office action dated August 12, 2003 have been considered. Claims 1-36 are pending in the application. Reconsideration and allowance of the application as amended is respectfully requested.

Claims 1-6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,978,902 to Mann (hereinafter *Mann*) in view of U.S. Patent No. 6,530,076 to Ryan et al. (hereinafter *Ryan*). The Applicant respectfully traverses the Examiner's rejection.

With respect to independent Claim 1, the Examiner contends that *Mann* discloses claimed recitations of Claim 1 including controllably designating at least one of a plurality of data collection periods defining temporal windows in which storage of the designated set of information is enabled, and storing the designated set of information identified by the designated information storage mode only during the temporal window corresponding to the designated data collection period. The Applicant respectfully disagrees with the Examiner's characterization of *Mann* as it pertains to at least these claimed features.

Mann is directed to a debug interface that uses a debug port (100) at a target system (101) to communicate with a host device (111). The host system is used to execute debug control software for transferring commands to the target system, and extracting and analyzing debug information generated by the target system (*e.g.*, col. 5, lines 1-4). *Mann* utilizes a test computer (*e.g.*, the host device 111) that is connected to the target device to debug the target device, where the host device sends commands including an information string to the operating system of the target device in order to extract information therefrom (*e.g.*, col. 3, lines 39-45).

To perform debugging according to *Mann*, a conventional "trace" function is used. *Mann* discloses that trace gathering is performed during selected sections of program execution (*e.g.*, col. 22, lines 13-16). With respect to starting and stopping trace capture, *Mann* states at column 22, lines 27-34:

> Various known methods are contemplated for enabling and disabling trace capture. For example, x86 commands are supplied for enabling and disabling the trace capture function. Alternatively, an existing x86 command is utilized to toggle a bit in an I/O port location. Furthermore, on-chip breakpoint control

registers (not shown) are configured to indicate the addresses at which trace capture is to start and stop.

As stated by the description in *Mann*, *Mann* utilizes known methods for enabling and disabling trace capture. The disclosed methods include sending commands from the host computer (111) to the target system (101) to directly control when the trace capture is to start and end.

The Examiner identifies column 22, lines 33-35 of *Mann* as teaching the controllable designation of at least one of a plurality of data collection periods defining temporal windows in which storage of the designated set of information is enabled. The cited portion of *Mann* indicates that on-chip breakpoint control registers are configured to indicate the addresses at which trace capture is to start and stop. Thus, as is known in conventional software program trace capturing, traces are executed between particular program instructions.

The present invention, on the other hand, allows for designation of operational events to define data collection periods. For example, as shown in FIGs. 6-7 and the corresponding description, a start event and a stop event may be controllably designated to identify particular operational events occurring in the computing system in which a temporal window for data capture is defined. For example, one exemplary start event is a "start on F/A compare" (FIG. 6, reference 608), which involves initiating writing data to the history stack when the current function and address match predefined function and address values (see page 27, line 21 through page 28, line 4). An example of a termination event is a "stop on EP detected critical error" (FIG. 7, reference 714) where the history stack stops writing to the history stack when a particular logic section (EP) sends an indication that a critical error occurred (see page 32, line 20 through page 33, line 3).

The conventional trace functions identified by the Examiner in *Mann* fail to teach or suggest the designation of operational events as identified in the Applicant's application that are used to designate data collection periods. The cited description in *Mann* merely indicates conventional trace activity where program addresses can be used to start and stop trace capture. Thus, *Mann* would be unable to perform data collection as described and claimed in the present invention. For example, with the present invention, a stop event may not occur until tens, hundreds, or millions of loop executions, and the present invention allows data

collection to stop when such a designated event occurs. The information stored will then show the state of the computing environment, in its normal operating environment, at the time of the stop event. With *Mann*, a program instruction breakpoint will simply run the program until the instruction breakpoint occurs, and the information that is relevant to the debugging may not be discovered.

In order to facilitate prosecution of this application, independent Claim 1 has been amended to restate this distinction using modified terminology. Claim 1 has been amended such that the designation of the data collection periods is based on operational events occurring in the computing system. The trace endpoints (*e.g.*, breakpoint) in *Mann* fails to disclose such claimed features.

The Examiner cited *Mann* in view of *Ryan* in the rejection of independent Claim 1. The Examiner has not established a showing that either *Mann* or *Ryan*, either alone or in combination, teaches or suggests any controllable designation of data collection periods. It is respectfully submitted that neither *Mann* nor *Ryan*, either alone or in combination, teach or suggest at least the claimed feature of Claim 1 to controllable designate at least one of a plurality of data collection periods based on operational events occurring in the computer environment.

To establish a *prima facie* case of obviousness based on a combination of references, three basic criteria must be met, as is set forth in M.P.E.P., §2143:

> 1) There must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;
> 2) There must be a reasonable expectation of success; and
> 3) The prior art references must teach or suggest all of the claim limitations.

Because neither *Mann* nor *Ryan*, either alone or in combination, teach or suggest at least the aforementioned feature of Claim 1, it is respectfully submitted that the Examiner's rejection of independent Claim 1 includes errors of finding of fact, which has led to a rejection that is grounded in an error of law. The Appellant respectfully submits that the resulting error of law compels reversal of the rejection of Claim 1, as *prima facie* obviousness is not established with respect to Claim 1, which is therefore allowable over the cited combination of references.

It is further noted that Claim 1 recited that at least one of a plurality of data collection periods are designated. In accordance with the present invention, a number of start and stop features (see FIGs. 6-7 and corresponding description) are established. Each combination of different start and stop events provides a different data collection period, and thus a plurality of such data collection periods are available. As set forth in Claim 1, one (or more) of these established data collection periods may be controllably designated as the desired data collection period. This is not taught in either *Mann* or *Ryan*, where instead a program instruction is simply set by the trace programmer. Neither *Mann* nor *Ryan* teach or suggest the presence of a plurality of data collection periods from which one or more may be designated. For this reason as well, it is respectfully submitted that the cited combination of references fails to "teach or suggest all of the claim limitations" of independent Claim 1. Again, the Applicant submits that the failure of the cited references to teach or suggest all of the claim limitations constitutes an error of finding of fact by the Examiner, which has led to an error of law compelling the reversal of the rejection of Claim 1.

The Examiner indicated that *Mann* fails to disclose controllably designating one of a plurality of information storage modes, wherein each of the information storage modes identifies a different set of information from the plurality of logical segments to be stored. The Examiner contends that *Ryan* discloses selectively tracing various processor signals, and alleges that this correlates to the controllable designation of one of a plurality of information storage modes as recited in Claim 1. The Applicant respectfully disagrees. For example, the Examiner identifies column 6, line 66 through column 7, line 2 as teaching this claimed feature. However, the Applicant points out that Claim 1 recites that each of a plurality of information storage modes identifies a different set of information from a plurality of logical segments in a computing system. Examples of such an arrangement are depicted in FIGs. 1 and 4 of the Applicant's patent application. *Ryan* does not teach this, but rather merely states that certain inputs from the processor 220 are selected to be traced. Thus *Ryan*, like *Mann*, relates to conventional instruction tracing, and *Ryan* does not teach sets of information from a plurality of logical segments in the computing environment. *Ryan* teaches only the tracing of the processor signals, and is silent with respect to identifying different sets of information provided from different logical segments within the computing environment. Similarly, the

Examiner identifies column 9, lines 16-18, lines 63-65, and FIG. 9 of *Ryan* as teaching the controllable designation of an information storage mode identifying a set of information. The recited portions of *Ryan* again refer to tracing functions associated with the processor signals, and therefore do not teach designating one of a plurality of information storage modes that each identify a different set of information from the plurality of logical segments to be stored.

It is respectfully submitted that *Ryan*, therefore, does not disclose the claimed features as purported by the Examiner to be taught by *Ryan*. *Mann* also fails to teach such features, and the Examiner does not indicate that *Mann* teaches such features. Neither *Mann* nor *Ryan*, either alone or in combination, teach the controllable designation of one of a plurality of information storage modes that identify different sets of information from a plurality of logic segments. Even assuming *arguendo* that *Mann* and *Ryan* were properly combined, the combination fails to teach or suggest the invention as claimed. For this additional reason, it is respectfully submitted that *prima facie* obviousness has not been established with respect to Claim 1.

To establish *prima facie* obviousness, the Examiner must also establish that there is some suggestion or motivation to combine the reference teachings, and that there is a reasonable expectation of success. The Applicant respectfully submits that this requirement has not been met. The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention to implement *Mann*'s tracing processor with selectively tracing various signals as in *Ryan*, providing a reason that "one of ordinary skill in the art would be motivated to record only required signals *to save processor work and memory space*." It is respectfully submitted that this rationale does not rise to the level of evidence of motivation as required by law.

There must be some objective reason to combine the teachings of the references. M.P.E.P § 2143.01. The Examiner's provided reason to combine *Mann* and *Ryan* is that it would "save processor work and memory space." The Examiner must explain the specific understanding or principle within the knowledge of one skilled in the art that would motivate one with no knowledge of the Applicant's invention to make the combination of references. *In re Rouffet*, 149 F.3d 1350, 47 USPQ.2d 1453 (Fed. Cir. 1998). Thus, the Examiner ostensibly argues that the specific principle of one skilled in the art that would motivate the artisan to

combine the references is to save processor work and memory space. It is respectfully submitted that the Examiner's proffered "motivation" represents a generic, conclusory statement that contains no specificity that would motivate a skilled artisan having no knowledge of the Applicant's invention to make the combination.

It is a requirement that actual evidence of a suggestion, teaching or motivation to combine prior art references be shown, and that this evidence be "clear and particular." *In re Dembiczak*, 50 USPQ2d 1614 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *In re Dembiczak.* The Applicant respectfully submits that the Examiner's speculative rationale "to save processing work and memory space" does not provide the actual, clear and particular evidence required to establish *prima facie* obviousness. For this reason as well, the Applicant maintains that *prima facie* obviousness has not been established, and Claim 1 is patentable over the cited combination of *Mann* and *Ryan.*

Dependent Claims 2-6, which are dependent from independent Claim 1, also stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Mann* in view of *Ryan.* While Applicant does not acquiesce with any particular rejections to these dependent claims, it is believed that these rejections are now moot in view of the remarks made in connection with independent Claim 1. These dependent claims include all of the limitations of Claim 1 and any intervening claims, and recite additional features which further distinguish these claims from the cited references. "If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious." M.P.E.P. §2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, dependent Claims 2-6 are also allowable over the combination of *Mann* and *Ryan.* Further, Claims 4 and 5 have been amended to more clearly indicate that at least one of a plurality of predetermined plurality of data collection commencement and termination events are designated, which is not taught nor suggested by *Mann* or *Ryan*, either alone or in combination.

Claims 7-18 and 23-34 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Mann*, in view of *Ryan*, and in further view of U.S. Patent No. 6,145,123 to Torrey et al. (hereinafter *Torrey*). The Applicant respectfully traverses the Examiner's rejection. Claim 7 is dependent from independent Claim 1. The Examiner has identified *Torrey* as teaching the

subject matter of Claim 7, relying on *Mann* and *Ryan* as teaching the subject matter of Claim 1 from which Claim 7 depends. *Torrey* does not teach or suggest the limitations of Claim 7 that are provided in its base claim (Claim 1), nor does the Examiner indicate that *Torrey* provides such a teaching. As indicated above, *Mann* and *Ryan* fail to teach or suggest the features provided in the base claim, and therefore a combination of *Mann*, *Ryan*, and *Torrey* fail to teach at least the features set forth in Claim 1, from which Claim 7 depends. Therefore, the combination of *Mann*, *Ryan*, and *Torrey* fail to teach or suggest all of the limitations of Claim 7, and Claim 7 is therefore allowable over the cited combination of references.

Further, it is respectfully submitted that the Examiner's stated motivation to combine the three references, *Mann*, *Ryan* and *Torrey*, does not rise to the level of actual, clear and particular evidence as required by the legal tenets previously set forth. The Examiner argues that one of ordinary skill in the art would be motivated to combine *Torrey* with *Mann* and *Ryan* because "Torrey is discussing a similar tracing processing system and both are using breakpoint registers." It is respectfully submitted that the combination of these references in an attempt to arrive at the claimed invention is made through impermissible hindsight, using the claimed invention as a blueprint for piecing together the prior art in an attempt to defeat patentability. (see *In re Dembiczak*). As recently stated by the Federal Circuit, "obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention." (*Crown Operations International, Ltd. v. Solutia Inc.*, 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002)). The Applicant respectfully submits that the general technological link of trace functions and use of breakpoints falls short of the requirement for actual, clear and particular evidence of the motivation to combine all of the *Mann*, *Ryan* and *Torrey* references. For this additional reason, it is respectfully submitted that *prima facie* obviousness has not been established with respect to Claim 7.

Claim 8, which is also dependent from Claim 1, also stands rejected as being obvious over *Mann* in view of *Ryan* and in further view of *Torrey*. The Applicant respectfully traverses the Examiner's rejection. The Examiner's reasons are stated as those used in connection with the rejections to Claims 4, 5, and 7. Amended Claim 8 is dependent from independent Claim 1. For the reasons set forth above in connection with independent Claim 1, *Mann* and *Ryan* fail to teach all of the limitations in Claim 1, from which Claim 8 depends.

Torrey does not teach or suggest the limitations of Claim 8 that are provided in its base claim (Claim 1), nor does the Examiner indicate that *Torrey* provides such a teaching. For at least this reason, it is respectfully submitted that the combination of *Mann*, *Ryan* and *Torrey* fail to teach or suggest all of the claim limitations of Claim 8, and fail to provide the requisite clear and particular evidence for motivation to combine such references. Therefore, *prima facie* obviousness has not been established with respect to Claim 8, and withdrawal of the rejection is respectfully requested.

Independent Claim 9 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Mann* in view of *Ryan* and in further view of *Torrey*. The Applicant respectfully traverses the Examiner's rejection. The Examiner summarily relies on the Examiner's arguments provided in connection with Claims 1, 4, 5, 7 and 8 as the basis for this rejection. The Applicant thus asserts that Claim 9 is allowable over the cited references for reasons provided above.

Further, the Applicant notes that Claim 9 includes: a memory for storing the operational information associated with the functional modules; a dynamically-configurable write mode selection module coupled to a control interface to receive one of a plurality of selectable write mode identifiers and to enable selected subsets of the operational information to be stored in the memory in response to the received write mode identifier; and a dynamically-configurable timing control module coupled to the control interface to receive one of a plurality of collection initiation identifiers and one of a plurality of collection termination identifiers, to enable storing of the selected subset of operational information into the memory upon activation of an initiation event corresponding to the received collection initiation identifier, and to terminate storing of the selected subset of operational information into the memory upon activation of a termination event corresponding to the received collection termination identifier. It is respectfully submitted that Claim 9 includes recited features different from those in Claims 1, 4, 5, 7 and 8, and the Examiner's rejection of Claims 1, 4, 5, 7 and 8 failed to address these different features. The Applicant has not been afforded an opportunity to respond, as the recited features of Claim 9 that differ from those of Claims 1, 4, 5, 7 and 8 were not addressed by the Examiner. The Applicant submits that *prima facie* obviousness has not been established, as the Examiner has not established that all

of the claimed limitations are taught or suggested by the combination of *Mann*, *Ryan*, and *Torrey*. For at least this reason, the Applicant respectfully requests that the rejection to independent Claim 9 be withdrawn, or the Examiner clarifies the rejection based on the language of Claim 9.

Claims 10, 11, 12 and 13 as originally filed were dependent on Claim 9. In the previous Office Action, the Examiner indicated that Claims 10-13 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 10-13 were rewritten in independent form, but are now rejected as being unpatentable over *Mann* in view of *Ryan* and in further view of *Torrey*. Therefore, Claims 10-13 include all the limitations of Claim 9, and recite additional features which further distinguish these claims from the cited references. For at least this reason, Claims 10-13 are in condition for allowance.

In addition, Claim 10 further recites that the dynamically-configurable write mode selection module comprises a write mode scan register that is loaded via a dynamic scan operation. The Examiner identifies *Torrey*, column 9, lines 31-35 as teaching the utilization of scan registers. The recited portion of *Torrey* states:

> The instruction trace configuration register (ITCR) may be accessed by either the serial/parallel interface or by a reserved opcode when X86 enhanced software debug mode is enabled. The developer must ensure that these two access modes are not used simultaneously.

As stated in the present Specification on page 35, lines 13-23:

> Generally, scan design approaches include an operation whereby certain desired logic patterns are serially inputted and shifted to the appropriate latch locations. Scan methods considers any digital circuit to be a collection of registers or flip-flops interconnected by combinatorial logic where data is then shifted into a large shift register organized from the storage elements of the circuit.... A dynamic scan operation is a scan operation where scanning may occur even where the system clock is operating, thereby eliminating the need to stop the system clock.

The Applicant respectfully submits that the recited portion of *Torrey* fails to teach such dynamic scan operations to load a write mode scan register according to the present invention, and therefore *prima facie* obviousness has not been established. This holds true for Claim 11

as well, which also recites the use of a dynamic scan operation, for loading a timing control scan register.

It is also noted that the Examiner's stated motivation to combine *Torrey* with *Mann* and *Ryan* for Claim 10 is that "one of ordinary skill in the art would be motivated to use a common method of register implementation." It is respectfully submitted that such a proffered motivation to combine falls well short of the actual, clear and particular evidence required to establish *prima facie* obviousness. For this additional reason, Claim 10 is in condition for allowance.

In addition, Claim 12 further recites a dynamically-configurable write mode selection module further comprising means for enabling the selected subset of the operational information to be stored in the memory if the subset of operational information changes from a first defined time to a second defined time, in response to a corresponding write mode selection identifier. The Examiner asserts that *Mann*, *Ryan* and *Torrey* further disclose this limitation, specifically indicating that *Ryan* teaches this claimed feature at column 2, lines 40-46 which states:

> Solving internal processor problems would be significantly eased if a mechanism were available to dynamically and selectively trace the various internal signals and operands in a processor and to record these dynamically selected signals and operands for later retrieval and analysis. This would significantly aid in solving processor problems

The Applicant respectfully submits that this does not teach or suggest the recited means for enabling the selected subset of the operational information to be stored in the memory if the subset of operational information changes from a first defined time to a second defined time, in response to a corresponding write mode selection identifier. The recited portion of *Ryan* mentions nothing about the means, nor has the Examiner established that the function associated with the means-plus-function claim corresponds to any function identified in *Ryan*. The recited portion of *Ryan* fails to indicate anything about a change of operational information from a first defined time to a second defined time, or to do so in response to a write mode selection identifier. For at least this additional reason, the rejection of Claim 12 should be withdrawn.

In addition, Claim 13 further recites a dynamically-configurable write mode selection module comprising means for enabling the selected subset of the operational information to be stored in the memory, if a current function value within the selected subset of operational information matches a predetermined function value, and if a current address value within the selected subset of operational information matches a predetermined address value, in response to a corresponding write mode selection identifier. The Examiner asserts that *Mann*, *Ryan* and *Torrey* further disclose this limitation, specifically indicating that *Mann* and *Torrey* teach this claimed feature at column 10, lines 15-67 (*Mann*) and columns 31-35 (*Torrey*). It is first noted that the *Torrey* patent document does not include such columns, and therefore it is unknown which portion of *Torrey* the Examiner refers to. With respect to *Mann*, the "functions" identified are *trace* functions or modes, and do not refer to function values of the computing environment to which comparisons and analyses are made. For this additional reason, the rejection to Claim 13 should be withdrawn.

Dependent Claims 14-18, which are dependent from independent Claim 9, were also rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of *Mann*, *Ryan* and *Torrey*. While Applicant does not acquiesce with the rejections to these dependent claims, it is believed that these rejections are now moot in view of the remarks made in connection with independent Claim 9. These dependent claims include all of the limitations of independent Claim 9 and any intervening claims, and recite additional features which further distinguish these claims from the cited references. If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. Therefore, dependent Claims 14-18 are also allowable over the combination of *Mann*, *Ryan* and *Torrey*. The Applicant reserves the right to argue any additional distinctions if the Examiner maintains the rejections to Claims 14-18.

Claim 23 as originally filed was dependent on Claim 9. In the previous Office Action, the Examiner indicated that Claim 23 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 23 was rewritten in independent form, but now stands rejected as being unpatentable over *Mann* in view of *Ryan* and in further view of *Torrey*. Therefore, Claim 23 includes all the limitations

of Claim 9, and recites additional features which further distinguish it from the cited references. For at least this reason, Claim 23 is in condition for allowance.

Dependent Claim 24 is dependent from independent Claim 23, and was also rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of *Mann*, *Ryan* and *Torrey*. While Applicant does not acquiesce with the rejection to this dependent claim, this rejection is moot in view of the remarks made in connection with independent Claim 23. Claim 24 includes all of the limitations of independent Claim 23, and recites additional features which further distinguish these claims from the cited references. Therefore, dependent Claims 14-18 are also allowable over the combination of *Mann*, *Ryan* and *Torrey*.

In addition, the Applicant points out that Claim 24 recites that at least one of the plurality of functional modules are external to the integrated circuit. The Examiner identifies *Mann*, particularly at column 7, lines 40-43, as teaching the feature recited in Claim 24. However, the recited portion of *Mann* clearly does not relate to a plurality of functional modules external to the integrated circuit as recited in Claim 24. As indicated in it's base claim (Claim 23), the plurality of functional modules are modules of the computing environment in which data is collected, *i.e.*, where each functional module is associated with time-varying operational information as each functional module operates. The recited portion of *Mann*, on the other hand, discloses two trace modes - an external and an internal mode. The external trace mode merely refers to a mode where trace records are sent to a trace port, and the internal mode refers to an internal trace buffer. These "modes" are trace storage modes, and do not relate at all to the functional modules of Claim 24 that refer to the functional modules producing the data that is being collected. For at least this additional reason, Claim 24 is in condition for allowance, and withdrawal of the rejection is respectfully requested.

Independent Claim 25 stands rejected as being unpatentable over *Mann* in view of *Ryan* and in further view of *Torrey*. The Applicant respectfully traverses the rejection. The Examiner states that the claim limitations of Claim 25 correspond to Claim 8, and therefore the rejection of Claims 1, 4, 5, 7 and 8 provide the rationale for rejecting Claim 25. The Applicant submits that Claim 25 is allowable over the cited combination of references for the reasons provided above, and incorporates those reasons here.

Dependent Claims 26-29 and 31-34 are dependent from Claim 25 and include the limitations of Claim 25 and any intervening claims. While the Applicant does not acquiesce with any of the particular reasons for rejection of these claims, these rejections are moot in view of the allowability of independent Claim 25. Therefore dependent Claims 26-29 and 31-34 are also in condition for allowance, and withdrawal of the rejections to these claims is respectfully requested.

Claim 30 as originally filed was dependent on independent Claim 25. In the previous Office Action, the Examiner indicated that Claim 30 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 30 was rewritten in independent form, but now stands rejected as being unpatentable over *Mann* in view of *Ryan* and in further view of *Torrey*. Therefore, Claim 30 includes all the limitations of Claim 25, and recites additional features which further distinguish it from the cited references. For at least this reason, Claim 30 is in condition for allowance.

In addition, Claim 30 includes reconfiguring the designated information storage mode to designate another one of the plurality of information storage modes, where reconfiguring the designated information storage mode includes dynamically scanning a storage mode identification into a scan register to designate the information storage mode. The Examiner identifies *Torrey*, column 9, lines 31-35 as teaching the utilization of scan registers. As previously indicated, this portion of *Torrey* states:

> The instruction trace configuration register (ITCR) may be accessed by either the serial/parallel interface or by a reserved opcode when X86 enhanced software debug mode is enabled. The developer must ensure that these two access modes are not used simultaneously.

This is clearly different, and does not teach or suggest, at least the dynamic scan operation as set forth in the present application. For at least this additional reason, *prima facie* obviousness has not been established with respect to Claim 30.

It is also noted that the Examiner's stated motivation to combine *Torrey* with *Mann* and *Ryan* for Claim 30 is that "one of ordinary skill in the art would be motivated to use a common method of register implementation." It is respectfully submitted that such a proffered motivation to combine falls well short of the actual, clear and particular evidence

required to establish *prima facie* obviousness. For this additional reason, Claim 30 is in condition for allowance.

The Applicant has addressed the lack of motivation to combine the cited references where the Examiner has identified some alleged motivation to combine *Mann* with *Ryan* and *Torrey*. For many claims, no specific motivation to combine references was identified by the Examiner. For such claims, it is respectfully submitted that *prima facie* obviousness has not been established, as no suggestion or motivation to combine such references for the respective claim has been provided. To the extent that the motivation to combine such references parallels the Examiner's interspersed assertions of a motivation to combine the cited references, the Applicant reiterates the aforementioned arguments that the stated motivation to combine *Mann*, *Ryan* and *Torrey* fails to provide the actual, clear and particular evidence required by law.

The Applicant notes the allowance of Claims 19-22, and thanks the Examiner for favorable consideration of these claims.

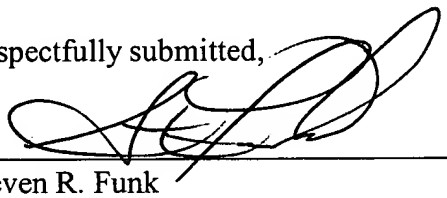
The Applicant also points out that Claims 35-36 were added to include embodiments where the designation of data collection periods is independent of the operational events occurring in the computing environment. For example, the "always on" start event (*e.g.*, FIG. 6, reference 606) can be used to provide an override commencement event such that the data collection is initiated upon initiating the "always on" feature. These newly added claims are fully supported by the Specification as originally filed, and no new matter has been added.

Finally, the Applicant points out that Claims 9-13, 19, and 23 have been amended, as the Applicant has discovered that the term "control interface" may have been inferentially claimed. These claims have been amended to affirmatively claim such control interface, and such amendments were not made in response to any of the Examiner's rejections, nor for any purposes of patentability. These amendments were made simply to comply with proper claim format. It is also noted that Claim 19 is currently allowed by the Examiner, however the Applicant has made this change to Claim 19 as well, in an effort to comply with proper claim drafting format. Further, Claim 25 was amended to simply make the language more clear. The breadth of these claims has not been narrowed through the amendments, nor has the Applicant intended to narrow the claims as a result of these amendments.

CONCLUSION

The Applicant respectfully submits that the pending claims are patentable over the cited prior art of record, and that the application is in condition for allowance. Authorization is given to charge Deposit Account No. 50-0996 (CRAWFORD) for the one-month extension of time. If the Examiner believes it necessary, the undersigned attorney of record may be contacted at (651) 686-6633 (x110) to discuss any issues related to this case.

Respectfully submitted,



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